SRINIVASA EDUCATIONAL SOCIETY'S

PACE INSTITUTE OF TECHNOLOGY & SCIENCES

(AUTONOMOUS)

Approved by AICTE, UGC, New Delhi & Govt. of Andhra Pradesh | Permanently Affiliated to JNTUK, Kakinada, A.P.

ACCREDITED BY **NAAC** WITH **'A'** GRADE | ACCREDITED BY **NBA**

An ISO 9001 : 2008 Certified Institution |'A' Grade Engineering College by Government of A.P.

NH-16, Near Valluramma Temple, ONGOLE - 523 272, A.P., Contact No.: 08592 278315, 9581456310 | www.pace.ac.in

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

MASTER OF TECHNOLOGY

IN

VLSI & ES

ACADEMIC REGULATIONS

AND

COURSE STRUCTURE & SYLLABI

(For the students admitted to

M.Tech Regular Two Years Programme from the Academic Year 2018-19

ACADEMIC REGULATIONS

For the students admitted to

M.Tech Regular Two Years Programme from the Academic Year 2018-19

ACADEMIC REGULATIONS R-18 FOR M.Tech (REGULAR)

(CHOICE BASED CREDIT SYSTEM)

Applicable for the students of M.Tech (Regular) from the Academic Year 2018-19

1. ELIGIBILITY CRITERIA FOR ADMISSION

The eligibility criteria for admission into M.Tech programme shall be as per the guidelines issued by the Andhra Pradesh State Council of Higher Education (APSCHE) and/or by any other competent authority.

2. PROGRAMMES OFFERED (POST GRADUATE)

A student shall be offered admission into any one AICTE-approved programme as given below:

S.No	PROGRAMME
01	Structural Engineering (SE)
02	Power Electronics (PE)
03	Machine Design (MD)
04	VLSI & Embedded Systems (VLSI&ES)
05	Computer Science and Engineering (CSE)

3. AWARD OF DEGREE

A student will be declared eligible for the award of M. Tech. degree, if he/she fulfils the following academic requirements:

i. 2 Year M.Tech Programme:

- The Student shall study a course for not less than two academic years and not more than four academic years.
- The student shall register for 68 credits and secure all the 68 credits.
- The students, who fail to fulfil all the academic requirements for the award of degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech Programme.
- No disciplinary action shall be in pending against the student by the time of the completion of his/her course. If any disciplinary action is pending against any student, he/she should not be awarded with the degree.

4. MEDIUM OF INSTRUCTION

The medium of instruction shall be English in all academic activities.

5. MINIMUM INSTRUCTION DAYS

The minimum instruction days for each Semester shall be 90.

6. CATEGORIZATION OF COURSES

The curriculum of each programme shall contain various courses indicated in the following categories to train the students for employment, higher learning, research and entrepreneurship.

i. **Professional Core (PC):** These courses are the core courses that provide the requisite foundation in the chosen Branch of Engineering.

ii. **Professional Elective (PE):** These courses are the elective courses opted by the students relevant to the chosen branch of engineering that provides the requisite foundation in a specific area of specialization.

iii. **Mandatory Courses (MC):** The Research Methodology and Intellectual Property Right is credit course relevant to the Research orientation.

iv. **Audit Courses (AC):** English for Research Paper Writing, Personality Development through Life Enlightenment Skills are non-credit courses relevant to the value education and also for enhancing employability skills.

7. CREDIT ASSIGNMENT

Each course is assigned a certain number of credits based on the following criteria.

Contact hours per week			
L	**T**	**P**	Credits
1	0	0	1
0	1	0	1
0	0	2	1

8. SEMESTER-WISE DISTRIBUTION OF CREDITS

The entire programme of study is for two academic years and is on semester pattern. The distribution of credits in each semester is as following.

Semester	Credits
I	23-25
II	23-25
III	08
IV	12
Total	**68**

9. ASSESSMENT AND EVALUATION

The performance of a student in each course shall be evaluated based on Continuous Internal Evaluation (CIE) and Semester End Examination (SEE) or only Continuous Internal Evaluation

S.No	Category of Course	Marks	
		CIE	SEE
1	Theory Courses	40	60
2	Laboratory Courses	40	60
3	Mandatory Courses	100	
4	Audit Courses	100	
5	Project Work Phase-I	50	--
	Project Work Phase-II	30	120

9.1 THEORY COURSES

9.1.1 Continuous Internal Evaluation (CIE):

Mid Term Examinations (40 Marks):

There shall be two mid-term descriptive examinations of 120 minutes each. The mid-term examinations shall be conducted with syllabi from units I,II & first half of III for the first mid and second half of III, IV & V units for the second mid. In each theory course, the question paper for the mid-term descriptive examination consists of four questions. A student is required to answer all four questions for maximum 40 marks.

CIE is computed as following: Finalized internal marks can be calculated with average of two mid term examinations marks and they shall be considered for marks of 40.

9.1.2 Semester End Examinations (SEE)

The semester end examinations for theory courses will be conducted covering all the units for 60 Marks. 5 Questions out of 8 Questions are to be answered of which each carries 12 Marks.

9.2 LABORATORY COURSES

9.2.1 Continuous Internal Evaluation (CIE)

The continuous internal evaluation for laboratory courses is based on the following parameters:

Parameter	Marks
Day-to-day Work	20
Internal Test	10
Record	05
Viva Voce	05
Total	40

9.2.2 Semester End Examinations (SEE)

The performance of the student in laboratory courses shall be evaluated jointly by internal and external examiners for 3 hours duration as per the parameters indicated below:

Parameter	Marks
Procedure/Algorithm	10
Experimentation/Program execution	15
Observations/Calculations/Testing	15
Result/Inference	10
Viva voce	10
Total	**60**

9.3 MANDATORY COURSES (CREDIT COURSES)

Mandatory courses are evaluated by the mode of a Presentation/ Comprehensive-Viva Voce/ Evaluation of Assignments. A student shall secure a minimum 50% of marks to get two credits. However, a student who secures less than 50 marks /abstains shall reappear in the subsequent semester(s).

9.4 **AUDIT COURSES (NON CREDIT COURSES)**

Audit courses are evaluated by the mode of a Presentation/ Comprehensive-Viva Voce/ Evaluation of Assignments. A student shall secure a minimum 50% of marks to get a satisfactory grade (SA). Otherwise unsatisfactory grade (US) will be indicated. However, a student who secures "US" grade /abstains shall reappear in the subsequent semester(s).

9.5 Project/Dissertation Work

Every candidate shall be required to submit a thesis or dissertation on a topic approved by the Project Review Committee.

i. A Project Review Committee (PRC) shall be constituted with Head of the Department and two other senior faculty members.

ii. Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses, both theory and practical upto II Semester.

iii. After satisfying 9.5 (ii), a candidate has to submit the project in consultation with his project supervisor, the title, objective and plan of action of his project work for approval. The student can initiate the project work, only after obtaining the approval from the Project Review Committee (PRC).

iv. If a candidate wishes to change his/her supervisor or topic of the project, he/she can do so with the approval of the Project Review Committee (PRC). However, the Project Review Committee (PRC) shall examine whether or not allow the change of topic/supervisor which may lead to a major change of his/her initial plans of project proposal. If yes, his/her date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

v. The work on the project shall be initiated at the begging of the II year and the duration of the project is two semesters.

vi. **Project Work (CIE) Assessment:**

- **Literature Review (CIE):**

  The performance of a student in project survey shall be evaluated by PRC within 8 weeks from the beginning of III Semester based on the following parameters:

Parameter	Marks
Literature Review	10
Presentation	05
Viva Voce	05
Total	20

- **Project Implementation-I (CIE):**

  The performance of a student in project implementation-I shall be evaluated at the end of III Semester. A student shall make a presentation on the project work Implementation-I before PRC. The evaluation criterion of review is based on the following parameters:

Parameter	Marks
Contribution	10
Innovation	10
Presentation	05
Viva Voce	05
Total	**30**

- **Project Implementation-II (Final) (CIE):**

  The performance of a student in project implementation-II (Final) shall be evaluated within 12 Weeks from the beginning of IV Semester. A student shall give a presentation on the final project work before PRC. The evaluation criterion of review is based on the following parameters:

Parameter	Marks
Contribution	10
Innovation	10
Presentation	05
Viva Voce	05
Total	**30**

vii. A candidate is permitted to submit the Project Thesis after satisfying the following conditions.

  a. Successful completion of theory and practical courses.

b. Not earlier than 40 weeks from the date of registration of the project work. The candidate has to pass all the theory and practical subjects before submission of the Thesis.

c. A student shall secure a minimum 50% of marks in CIE to award as satisfactory grade (SA). Otherwise unsatisfactory grade (US) will be indicated. However, a student who secures "US" grade /abstains shall reappear in the subsequent semester(s).

d. A candidate shall publish his/her project work in a reputed journal.

e. A candidate shall take approval of PRC.

viii. Four copies of the Project Thesis certified by the Supervisor shall be submitted to the Institute.

ix. The thesis shall be adjudicated by an External Examiner approved by the Principal from a panel of 4 Examiners who are eminent in the field, submitted by the Department. The Head of the Department shall coordinate and make arrangements for the conduct of Viva Voce examination.

x. **Project Work Viva Voce (SEE) Assessment:**

A student shall submit a duly-certified project report to the department in a specified time. He/She shall give presentation on the project work before the board consisting of the Supervisor, the Head of the Department and the examiner who adjudicated the Thesis. The performance of the student is evaluated as per the following parameters:

Parameter	Marks
Project report	40
Innovation	30
Presentation	20
Viva Voce	15
Research Publication (Seminar/Conference/Symposium/Journal)	10
Scope of Implementation	05
Total	**120**

- **AWARD OF LETTER GRADES**

A letter grade and grade points shall be awarded to a student based on his/her performance in Project Viva Voce (120 M) as given below.

% Marks	Marks	Letter Grade	Level
≥ 90	≥ 108	A	Outstanding
70 to <90	84 to <108	B	Excellent
50 to <70	60 to <84	C	Good
<50	<60	F	Fail
--	--	Ab	Absent

A student who secures "F" grade in any course shall be considered "Failed" and is required to reappear as "Supplementary student" in SEE, as and when offered. In such cases, his/her CIE marks in those courses will remain same as obtained earlier. A student, who is absent for any examination shall be treated as "Failed".

If the report of the examiner is favorable, Viva-Voce examination shall be conducted by the board consisting of the Supervisor, the Head of the Department and the examiner who adjudicated the Thesis. The board shall jointly report the candidate's work as one of the following:

A: Excellent

B: Good

C: Satisfactory

D: Unsatisfactory

vi. If the report of the Viva-Voce is unsatisfactory, the candidate shall retake the Viva Voce examination only after three months. If he/she fails to get a satisfactory report at the second Viva-Voce examination, the candidate has to re-register for the project and complete the project within the stipulated time after taking the approval from the PRC.

10. ATTENDANCE REQUIREMENTS

a. A student is eligible to write the Semester End Examinations if he acquires a minimum of 75% of attendance in aggregate of all the subjects.

b. Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee on medical grounds.
c. A stipulated fee shall be payable towards condonation of shortage of attendance.
d. If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.
e. Shortage of Attendance below 65% in aggregate shall not be condoned.
f. A student who is shortage of attendance in semester may seek re-admission into that semester when offered within one week from the date of the commencement of class work.
g. Students whose shortage of attendance is not condoned in any semester are not eligible to write their Semester End Examination of that class.

11. MINIMUM ACADEMIC REQUIREMENTS

The following academic requirements have to be satisfied in addition to the attendance requirements mentioned in item no.10.

a. A student shall be deemed to have satisfied the minimum academic requirements, if he/she gains the credits allotted to each course and secures not less than a minimum 40% of marks exclusively at the Semester End Examination. However, the student should secure minimum 50% of marks in both CIE and SEE put together to be eligible for passing the course.
b. The Students, who fail to earn 68 credits as indicated in the course structure within 4 academic years from the year of admission, shall forfeit their seat in M.Tech programme and admission stands cancelled.

12. PROCEDURES FOR SEMESTER END EXAMINATIONS

i. **Supplementary examinations:** There shall be supplementary examinations along with regular semester end examinations for a student to reappear in the course(s) he/she failed or not attempted.
ii. **Recounting:** A student, who wishes to verify the total marks obtained by him/her in any theory course in SEE can apply for recounting in response to the notification along with the prescribed fee. The outcome of the recounting gets reflected in the results sheet and grade card.

iii. **Revaluation:** A student who wishes to apply for revaluation of a theory course in SEE can submit an application along with the prescribed fee as per the notification issued.

a. If the variation in marks of the first valuation and revaluation is ≤ 15% of the total marks, then the better of the two evaluations shall be considered as final marks.

b. If the variation of marks between the first valuation and revaluation is >15% of the total marks, there shall be a third evaluation by another examiner. The average marks of two nearer evaluations shall be taken into consideration. In case of any fractional value of marks, it can be rounded off to the next integer value.

c. If a student secures a higher grade in the revaluation, that grade will be declared as the final grade. Otherwise, the original grade will remain valid.

13. AWARD OF LETTER GRADES

A letter grade and grade points shall be awarded to a student in each course based on his/her performance as per the 10-point grading system given below.

Marks (Max:100)	Letter Grade	Grade Point	Level
≥ 90	O	10	Outstanding
80 to <90	S	9	Excellent
70 to <80	A	8	Very Good
60 to <70	B	7	Good
50 to <60	C	6	Pass
<50	F	0	Fail
--	Ab	0	Absent

Marks (Max:100)	Letter Grade	Grade Point	Level
≥ 50	SA	-	Satisfactory
< 50	US	-	Unsatisfactory
--	Ab	-	Absent

a. A student who secures "F" grade in any course shall be considered "Failed" and is required to reappear as "Supplementary student" in SEE, as and when offered. In such cases, his/her CIE marks in those courses will remain same as obtained earlier.

b. A student, who is absent from any examination shall be treated as "Failed".

c. In general, a student shall not be permitted to repeat any course (s) for the sake of "Grade improvement" or "SGPA/CGPA improvement".

14. COMPUTATION OF SGPA & CGPA

a. Semester Grade Point Average (SGPA)

The performance of each student at the end of each semester is indicated in terms of SGPA. The SGPA is the ratio of sum of the product of the number of credits and the grade points scored by a student in all the courses to the sum of the number of credits of all the courses.

$$\mathbf{SGPA\ (S_i) = \Sigma\ (C_i \times G_i) / \Sigma C_i}$$

Where C_i is the number of credits of the i^{th} course and G_i is the grade point scored by the student in the i^{th} course.

b. Cumulative Grade Point Average (CGPA)

The CGPA is a measure of the overall cumulative performance of a student. The CGPA is calculated in the same manner taking into account all the courses undergone by a student over all the semesters of a programme.

$$\mathbf{CGPA = \Sigma\ (C_i \times S_i) / \Sigma C_i}$$

Where S_i is the SGPA of the i^{th} semester and C_i is the total number of credits in that semester.

c. The SGPA and CGPA are rounded off to 2 decimal points and reported in grade cards.

15. AWARD OF CLASS

A student who satisfies the minimum requirements prescribed for the completion of a programme is eligible for the award of M.Tech degree and he/she shall be placed in one of the following four classes on a 10 point scale.

Class Awarded	CGPA to be secured	From the CGPA secured from 68 Credits
First Class with Distinction	≥ 7.5 with no subject failures	
First Class	≥ 6.5 with subject failures	
Second Class	≥ 5.5 to < 6.5	
Pass Class	> 5.0	

16. DISCIPLINE

a. A student is required to observe discipline and decorum both inside and outside the college and not to indulge in any activity that may tarnish the prestige of the college. The head of the institution shall constitute a disciplinary committee to enquire into acts of indiscipline and notify the college about the disciplinary action taken. In case of any serious disciplinary action, which leads to suspension or dismissal, a committee shall be constituted by head of the institution for taking final decision.

b. Those students who indulge in examination related malpractices shall be punished as per the scale of punishment notified in Annexure-I.

c. Those students involved in the illegal acts of ragging shall be punished as per the provisions of Act 26, 1997 of Govt. of Andhra Pradesh (Annexure-II).

17. REVISION OF REGULATIONS, CURRICULUM AND SYLLABI

The college may revise, amend or change the regulations, curriculum, syllabus and scheme of examinations from time to time subject to decisions/recommendations of Board of Studies and the College Academic Council.

18. WITHHOLDING OF RESULTS

If a student fails to clear dues, if any, payable to the institution or any case of indiscipline is pending against him, the result of the student will be withheld, and also the award of his/her degree shall be withheld in such cases.

19.TRANSITORY REGULATIONS

a. A student, who is detained or discontinued in the semester, on readmission shall be required to do all the courses in the curriculum prescribed for the batch of students in which the student joins

subsequently. However, exemption will be given to those students who have already passed the courses in the earlier semester(s) he/she is originally admitted into and substitute courses are offered in place of them as approved by the Board of Studies.

b. In general, after transition, there will be a fitment formula approved by the competent authority in order to balance course composition and the number of credits.

c. Students admitted by transfer from other institutions shall follow transitory regulations with suitable fitment formulae approved by the competent authority.

d. A student who is seeking readmission shall apply in the prescribed format within one week after the commencement of the class work. However, the readmission of a student shall be approved by the competent authority.

20.COURSE CODE

The Course Codes will be given by the departments concerned to the subject. Each course code contains 8 characters. The 8 characters for each subject will be filled as per the following description:

1	2	3	4	5	6	7	8	9

1 Character : Institute Name as '**P**"

2 Character : Post Graduation Name as '**P**"

3,4 Characters: Year of Commencement of Regulations as '**18**'

5,6 Characters: Subject/Branch Category such as

CE for Civil Engineering Courses

EE for Electrical & Electronics Engineering Courses

ME for Mechanical Engineering Courses

EC for Electronics & Communication Engineering Courses

CS for Computer Science & Engineering Courses

MC for Mandatory Courses

7 Character: Mode of Subject Learning and Evaluation such as

T for Theory Courses

L for Laboratory Courses

S for Seminar

P for Project

M for Mini Project

V for Viva Voce

E for Professional Elective Courses

O for Open Elective Courses

A for Audit Course

8,9 Characters: Serial number of the course taught by the department in that Semester such 01, 02, 03,..... etc

21. GENERAL

- Wherever the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".
- The academic regulations should be read as a whole for the purpose of any interpretation.
- In case of any doubt or ambiguity in the interpretation of the above rules, decision of the competent authority is final and binding.
- The college may change or amend academic regulations or syllabi at any time subject to approval of the competent authority and the changes or may apply the amendments made to all students with effect from the dates notified.

22. STATUTORY DECLARATION

In case the regulations do not specify application of an appropriate rule in a unique case, the decision of the competent authority of the college shall be final.

******

ANNEXURE-I

MALPRACTICE RULES

DISCIPLINARY ACTION FOR MALPRACTICE/IMPROPER CONDUCT IN EXAMINATIONS

S.No	Nature of Malpractices/Improper Conduct	Punishment
1 (a)	If a student possesses or tries to access any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	If a student gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	If a student is found to have copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work, and shall not be permitted to appear for the remaining examinations of the subjects of that Semester. The Hall Ticket of the candidate is to be cancelled.
3.	Impersonates any other candidate in connection with the examination	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate, who has been impersonated, shall be cancelled in all the subjects of the Examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all Semester End Examinations. The

		continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is to be registered against him.
4.	If a student smuggles inside the exam hall an Answer book or additional sheet or takes out or Arranges to send out the question paper or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and all Semester End Examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	If a student uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in the subject.
6.	If a student refuses to obey the orders of the Chief Superintendent/Controller of Examinations / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	Such a student(s) shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester. The candidates also are to be debarred and forfeited their seats. In case of outsiders, they will be handed over to the police and a police case is to be registered against them.

7.	If a student leaves the exam hall taking away answer script or intentionally tears the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also debarred for two consecutive semesters from class work and Semester End Examinations. The continuation of the course by the candidate is subjected to the academic regulations in connection with forfeiture of the seat .
8.	If a student possesses any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also to be debarred and forfeited the seat.
9.	If a student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student shall be expelled from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester. The candidate is also to be debarred and forfeited the seat. Person(s) who do not belong to the College will be handed over to police and, a police case shall be registered against them.
10.	If a student comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester.
11.	If copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester examinations.

Malpractices identified by squad or special invigilators

- Punishments to the candidates are as per the above guidelines.
- Punishment to institutions : (if the squad reports that the college is also involved in encouraging malpractices)
    i. A show cause notice shall be issued to the college.
    ii. Impose a suitable fine on the college.
    iii. Shifting the examination centre from the college to another college for a specific period of not less than one year.

ANNEXURE-II

Prohibition of ragging in educational institutions Act 26 of 1997

Salient Features

- Ragging within or outside any educational institution is prohibited.
- Ragging means doing an act which causes or is likely to cause Insult or Annoyance of Fear or Apprehension or Threat or Intimidation or outrage of modesty or Injury to a student

	Imprisonment upto		Fine Upto
Teasing, Embarrassing and Humiliation	6 Months	+	Rs. 1,000/-
Assaulting or Using Criminal force or Criminal intimidation	1 Year	+	Rs. 2,000/-
Wrongfully restraining or confining or causing hurt	2 Years	+	Rs. 5,000/-
Causing grievous hurt, kidnapping or Abducts or rape or committing unnatural offence	5 Years	+	Rs. 10,000/-
Causing death or abetting suicide	10 Years	+	Rs. 50,000/-

In Case of Emergency CALL TOLL FREE NO. : 1800 - 425 - 1288

ABSOLUTELY NO TO RAGGING

1. Ragging is prohibited as per Act 26 of A.P. Legislative Assembly, 1997.
2. Ragging entails heavy fines and/or imprisonment.
3. Ragging invokes suspension and dismissal from the College.
4. Outsiders are prohibited from entering the College and Hostel without permission.
5. Girl students must be in their hostel rooms by 7.00 p.m.
6. All the students must carry their Identity Cards and show them when demanded
7. The Principal and the Wardens may visit the Hostels and inspect the rooms any time.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

R18 Regulations M. Tech. (VLSI & ES) Course Structure

I YEAR I SEMESTER								
S.No	**Course Code**	**Course Name**	**L**	**T**	**P**	**Credits**	**Internal**	**External**
1	PP18ECT01	Digital System Design	3	1	0	4	40	60
2	PP18ECT02	CMOS Analog & Digital IC Design	3	1	0	4	40	60
3	PP18ECT03	VLSI Technology and Design	3	0	0	3	40	60
4	PP18ECT04	Microcontrollers For Embedded System Design	3	0	0	3	40	60
5	**Professional Elective -I**		3	0	0	3	40	60
	PP18ECE01	Advanced Digital Design using Verilog HDL						
	PP18ECE02	Nano Electronics						
	PP18ECE03	ASIC Design						
	PP18ECE04	CPLD & FPGA architecture						
6	**Professional Elective -II**		3	1	0	4	40	60
	PP18ECE05	Semiconductor Memory Design and Testing.						
	PP18ECE06	Hardware Software Co-Design						
	PP18ECE07	Embedded Networking						
	PP18ECE08	Advanced Operating Systems						
7	PP18ECA01	English for Research Paper Writing	2	0	0	0	-	-
8	PP18ECL01	VLSI LAB	0	0	3	1.5	40	60
Total			**20**	**3**	**3**	**22.5**	**280**	**420**

I YEAR II SEMESTER								
S.No	**Course Code**	**Course Name**	**L**	**T**	**P**	**Credits**	**Internal**	**External**
1	PP18ECT05	Real Time Operating System	3	0	0	3	40	60
2	PP18ECT06	Test and Testability	3	1	0	4	40	60
3	PP18ECT07	Wireless Sensor Networks	3	1	0	4	40	60
4	PP18ECT08	Network Security And Cryptography	3	1	0	4	40	60
5	**Professional Elective -III**		3	0	0	3	40	60
	PP18ECE09	IoT & Applications						
	PP18ECE10	Advanced Digital Signal Processing						
	PP18ECE11	Physical Design Automation						
	PP18ECE12	Mobile Smart Communication Devices						
6	**Professional Elective -IV**		3	1	0	4	40	60
	PP18ECE13	Image & Video Processing						
	PP18ECE14	Embedded Device Drivers						
	PP18ECE15	VLSI Signal Processing						
	PP18ECE16	Artificial Intelligence						
7	PP18ECA02	Personality Development through Life Enlightenment Skills	2	0	0	0	-	-
8	PP18ECL02	Embedded System Design LAB	0	0	3	1.5	40	60
Total			**20**	**4**	**3**	**23.5**	**280**	**420**

II YEAR I SEMESTER								
S.No	**Course Code**	**Course Name**	**L**	**T**	**P**	**Credits**	**Internal**	**External**
1	PP18MCT01	Research Methodology and IPR	2	0	0	2	100	-
2	PP18ECP01	Project Work Phase-I	0	0	0	8	50	-
Total			**2**	**0**	**0**	**10**	**150**	**-**

II YEAR II SEMESTER								
S.No	**Course Code**	**Course Name**	**L**	**T**	**P**	**Credits**	**Internal**	**External**
1	PP18ECP02	Project Work Phase-II	**0**	**0**	**0**	12	30	120
Total			**0**	**0**	**0**	**12**	**30**	**120**

M.Tech. I Year I Sem

Course Structure

L	T	P	C
3	1	0	4

DIGITAL SYSTEM DESIGN

Internal Marks: 40

Course Code: PP18ECT01 **External Marks:** 60

Course Prerequisite: Digital Circuits

Course Objectives:

Students will try to learn:

1. To understand CAMP algorithms.
2. To understand characteristics of memory and their classification.
3. To understand concepts of sequential circuits and to analyze sequential systems in terms of state machines.
4. To understand concepts of fault modeling and test pattern.
5. To implement fault detection methods.

Course Outcomes:

After successful completion of the course student will be able to

1. Develop a digital logic and apply it to solve real life problems.
2. Develop different semiconductor memories and binary arithmetic.
3. Analyze, design and implement sequential logic circuits.
4. Analyze fault detection and testing.
5. Simulate and implement fault detection methods of sequential circuits.

UNIT-I (10 Lectures)

Minimization Procedures and CAMP Algorithm:

Review on minimization of switching functions using tabular methods, k-map, and QM algorithm

CAMP-I algorithm, Phase-I:

Determination of Adjacencies, DA, CSC, SSMs and EPCs, CAMP- I algorithm, Phase-II: Passport checking, Determination of SPC

CAMP-II algorithm:

Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II (9 Lectures)

PLA Design, PLA Minimization and Folding Algorithms

Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT -III (9 Lectures)

Design of Large Scale Digital Systems:

Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV (10 Lectures)

Fault Diagnosis in Combinational Circuits:

Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V (10 Lectures)

Fault Diagnosis in Sequential Circuits:

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

Text Books:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi , 2nd Edition, 2001, TMH
3. Digital system Design using PLDd-Lala

Reference Books:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Son Inc.

Web Reference:

1. https://drive.google.com/file/d/1ka6HEHdCxq5hpoyK7vGTxzXfweymGfMR/view?usp=sharing
2. http://ee.sharif.edu/~asic/Lectures/Lecture_06_FPGA.pdf
3. https://drive.google.com/file/d/1DcFUopD_kou_l1P_bcna3ArG8oMAaaDs/view?usp=sharing
4. https://drive.google.com/file/d/1mhQXBP7P4p6IyGt3sKNKpKPqSiRhtsa7/view?usp=sharing
5. http://www.ece.utep.edu/courses/web5375/Notes_files/ee5375_fault_modeling.pdf

M.Tech. I Year I Semester

Course Structure

L	T	P	C
3	1	0	4

CMOS ANALOG AND DIGITAL IC DESIGN

Internal Marks: 40

Course Code: PP18ECT02 **External Marks: 60**

Course Prerequisite: STLD& IC Design

Course Objectives:

1. Acquire knowledge on the large and small signal models for analog design in CMOS technology including MOSFET models,
2. Understand current Mirror and Wilson Current Mirror circuits
3. Acquire knowledge on amplifiers (single-/multi-stage, differential and operational) in CMOS technology,
4. Understand the different logic circuit designs for logic expressions and the importance of the circuit designs,
5. Understand the designs both in combinational as well as sequential.

Course Outcomes:

The Students at the end of the course must be able to:

1. Describe the large and small signal models for analog design in CMOS technology including MOSFET models.
2. Analyze current mirrors and voltage references taking supply, temperature and process variations into account.
3. Analyze amplifiers (single-/multi-stage, differential and operational) in CMOS technology.
4. Realize the different logic circuit designs for logic expressions and the importance of the circuit designs.
5. Understand the designs both in combinational as well as sequential.

UNIT –I (9 Lectures)

MOS Devices and Modeling:

The MOS Transistor, Passive Components-Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT –II (10 Lectures)

Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascade current

Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures. Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps.

UNIT-III (9 Lectures)

MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-IV (10 Lectures)

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design.CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-V (10 Lectures)

Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Text Books:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg,Oxford University Press, International Second Edition/Indian Edition,2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, PaulJ. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.
3. Digital Integrated Circuit Design – Ken Martin, Oxford University Press,2011.
4. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, WileyStudent Edn, 2013.
2. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

Web Reference:

1. https://books.google.co.in/books?isbn=0199937427
2. https://books.google.co.in/books?isbn=047137752X
3. https://books.google.co.in/books?isbn=0195125843
4. https://books.google.co.in/books?isbn=0070530777
5. https://books.google.co.in/books?isbn=8126517786
6. https://books.google.co.in/books?isbn=143986859X

M.Tech. I Year I Semester

Course Structure

L	T	P	C
3	0	0	3

VLSI TECHNOLOGY AND DESIGN

Internal Marks: 40

Course Code: PP18ECT03 **External Marks: 60**

Course Prerequisite: Basics of VLSI

Course Objectives:

1. To learn the basic MOS Circuits
2. To learn the MOS Process Technology
3. To understand the operation of MOS devices.
4. To understand the Layout process and standard design rules.
5. To learn the floor planning and chip design fundamentals.

Course Outcomes:

1. Understand the fabrication process of IC technology
2. Analysis of the operation of MOS transistor
3. Analysis of the physical design process of VLSI design flow
4. Able to analyzing of the design rules and layout diagram of complex problems.
5. Understand the floor planning and chip design methodologies.

UNIT-I (10 Lectures)

VLSI Technology:

Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

VLSI Design:

Electronic design automation concept, ASIC and FPGA design flows,SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-II (10 Lectures)

CMOS VLSI Design:

MOS Technology and fabrication process of PMOS, NMOS, CMOS and BiCMOS technologies**,** comparison of different processes.

Building Blocks of a VLSI circuit:

Computer architecture, memory architectures, communication interfaces, mixed signal interfaces.

VLSI Design Issues:

Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT-III (9 Lectures)

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitatitive

and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-IV (9 Lectures)

Subsystem Design and Layout:

Some architectural issues switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.

Subsystem Design Processes:

Some general considerations and an illustration of design processes, design of an ALU subsystem

UNIT-V (10 Lectures)

Floor Plan:

Design Styles and specific issues, Estimating Cost of Floor plan, Slicing Structure, A Hierarchical Floor Plan.

Architecture Design:

Introduction, Register-Transfer design, high-level synthesis, architectures for low power, architecture testing.

Chip Design:

ESD Protection, Input Circuits, Output Circuits, On-chip clock Generation and Distribution, Latch-up and its prevention.

Text Books:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian, Douglas A. Pucknell, SholehEshraghian, 2005, PHI Publications.
2. Modern VLSI Design-Wayne Wolf, 3rd Ed., 1997, Pearson Education.
3. CAD for VLSI Circuits- By Experienced Faculty, JNTUK, Professional Publications (2014)

Refernce Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming-BO Lin,CRC Press, 2011.
2. Principals of CMOS VLSI Design-N.H.E Weste, K. Eshraghian, 2nd Edition, Addison Wesley.

Web Reference :

1. https://nptel.ac.in/courses/117101058/
2. https://www.class-central.com/tag/vlsi%20design
3. https://www.coursera.org/learn/vlsi-cad-logic#syllabus
4. https://www.coursera.org/learn/vlsi-cad-layout?siteID=.GqSdLGGurk-6YUt3I9x0L_FDx.vKzxPkA&utm_content=10&utm_medium=partners&utm_source=linkshare&utm_campaign=*GqSdLGGurk

M.Tech. I Year I Sem **Course Structure**

L	T	P	C
3	0	0	3

MICRO CONTROLLERS FOR EMBEDDED SYSTEM DESIGN

Internal Marks: 40

Course Code: PP18ECT04 **External Marks:** 60

Course Prerequisite: Micro Processors and advanced Micro controllers

Course Objectives:

1. To understand the design aspects of ARM processors.
2. Basic introduction for programming on ARM processor
3. Able to understand C programming using for ARM processor
4. To describe various cache-technologies that surrounds the ARM cores.

Course Outcomes:

Upon completion of the course students will be able to

1. Understand and analyze the design aspects, Architecture, and instruction set associated with ARM processors.
2. Analyze the C programming optimization methods for ARM processor
3. Examines various cache-technologies that surround the ARM cores.

UNIT-I (9 Lectures)

ARM Architecture - ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families.

UNIT II (10 Lectures)

ARM Programming Model-I - Instruction Set: Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT III (10 Lectures)

ARM Programming Model-II - Thumb Instruction Set: Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions

UNIT IV (10 Lectures)

ARM Programming - Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops.

UNIT V (9 Lectures)

Memory Management - Cache Architecture, Polices, Flushing and Caches, MMU, Page Tables, Translation, Access Permissions, Content Switch.

Text Books:

1. Andrew Sloss, Dominic Symes, Chris Wright, “ARM system Developers Guide: Designing and Optimizing System Software”, Elsevier publications, 2004.

Reference Books:

1. Valvano, J. (2011),”Embedded microcomputer systems: real time interfacing”, 3rd Edition, Cengage Learning.

Web Reference:

1.https://www.arm.com/products/processors

2.https://developer.arm.com/products/architecture/cpu-architecture

3.https://en.wikipedia.org/wiki/ARM_architecture

4.https://www.cs.ccu.edu.tw/~pahsiung/courses/ese/.../ESD_03_ARM_Architecture.pdf

M.Tech. I Year I Semester

Course Structure

L	T	P	C
3	0	0	3

ADVANCED DIGITAL DESIGN USING VERILOG HDL

(Professional Elective -I)

Internal Marks: 40

Course Code: PP18ECE01 **External Marks: 60**

Course Prerequisite: Basic of digital Circuits, Introduction to VHDL

Course Objectives:

1. Gain knowledge on sequential machines and behavioral modeling.
2. Acquire knowledge on synthesis of combinational and sequential logics.
3. Gain knowledge on design and synthesis of data path controllers.
4. Gain knowledge on algorithms and architectures of digital processors.
5. Gain knowledge on estimation of design and timing validations.

Course Outcomes:

Upon the completion of this course, students will be able to

1. Demonstrate in-depth knowledge in sequential machine design and modeling.
2. Design and synthesize combinational and sequential logic.
3. Able to demonstrate algorithms and architectures of DSPs.
4. Develop architectures for processors and controllers.
5. Apply post synthesis design tasks for any design.

UNIT-I (10 Lectures)

Introduction to Digital Design Methodology:

Glitches and Hazards,Design of sequential machines, state-transition graphs, design example:BCD to Excess-3 code converter, serial - line code converter for data transmission, state reduction, and equivalent states, Algorithmic State Machine Charts for behavioral modeling, ASMD charts, switch debounce, metastability, and synchronizers for asynchronous signals, design example: keypad scanner and encoder.

UNIT-II (10 Lectures)

Synthesis of Combinational and Sequential Logic:

Introduction to synthesis, synthesis of combinational logic, synthesis of sequential logic with flip-flops, synthesis of explicit state machines, registered logic, state encoding, synthesis of implicit state machines, registers, and counters, synthesis of gated clocks and clock enables

UNIT-III (10 Lectures)

Design and Synthesis of Datapath Controllers:

Partitioned sequential machines, design example: binary counter, design and synthesis of a RISC stored-program machine, design example: UART

UNIT-IV (9 Lectures)

Algorithms and Architecture for Digital Processors:

Algorithms, nested-loop programs, and data flow graphs, digital filters and signal processors, building blocks for signal processors, asynchronous FIFOs synchronization across clock domains.

UNIT-V (9 Lectures)

Post synthesis Design Tasks:

Post synthesis design validation, post synthesis timing verification, estimation of ASIC timing violations, false paths, system tasks for timing verification.

Text Books:

1. Michael D. Ciletti (2002), "Advanced digital design with the Verilog HDL", Eastern economy edition, PHI.

Reference Books:

1. Stephen Brown & Zvonko Vranesic (2007) , "Fundamentals of Digital logic with Verilog design", 2nd edition, Tata McGraw Hill,.
2. Ian Grout (2011), "Digital systems design with FPGAs and CPLDs",Elsevier Publications.
3. Palnitkar, S. (2003). Verilog HDL: a guide to digital design and synthesis (Vol. 1). Prentice Hall Professional.

Web Reference:

1. http://web.uettaxila.edu.pk/CMS/coeADDbsSp09/notes%5CLecture%203,4.pdf
2. https://lecturenotes.in/notes/15437-digital-design-through-verilog-hdl-ddtv-by-vtu-rangers
3. https://www.smartzworld.com/notes/digital-design-through-verilog-hdl-notes-ddtv/

M.Tech. I Year I Semester

Course Structure

L	T	P	C
3	0	0	3

NANO ELECTRONICS

(Professional Elective -I)

Internal Marks: 40

Course Code: PP18ECE02 **External Marks: 60**

Course Prerequisite: Semi Conductor Physics, Electronics Devices

Course Objectives:

1. To introduce the students to nano electronics, nano devices, spintronics and molecular electronics.
2. To identify quantum mechanics behind nanoelectronics.
3. To describe the principle and the operation of nano electronic devices.
4. To tell about applications of nano electronics.
5. To explain the principle and application of spintronic devices.

Course Outcomes:

1. Know the nano electronics holds the capacity for mass production of high-quality nano devices with an enormous variety of applications from computers to biosensors, from cell phone to space shuttles and from large display screens to small electronic toys.
2. Student will know the scaling of transistors and other devices to smaller and smaller sizes, which has provided the basis for this exponential growth, has limits, physical (size of the atoms), technological (lithography) and economic, which will be reached by nano electronics in the next coming decade.
3. Differentiate between microelectronics and nano electronics.
4. Understand the impact of nano electronics onto information technology, communication and computer science.
5. Describe the spin-dependant electron transport in magnetic devices.

UNIT-I (10 Lectures)

Single-electron and few-electron phenomena and devices: Tunnel junction and applications of tunneling, Tunneling Through a Potential Barrier, Potential Energy Profiles for Material Interfaces, Metal—Insulator, Metal-Semiconductor, and Metal-Insulator-Metal Junctions.

UNIT-II (9 Lectures)

Applications of Tunneling; Field Emission, Gate—Oxide Tunneling and Hot Electron Effects in MOSFETs, Theory of Scanning Tunneling Microscope, Double Barrier Tunneling and the Resonant Tunneling Diode.

UNIT-III (8 Lectures)

Coulomb Blockade: Coulomb Blockade, Coulomb Blockade in a Nano capacitor, Tunnel Junctions, Tunnel Junction Excited by a Current Source, Coulomb Blockade in a Quantum Dot Circuit.

UNIT-IV (10 Lectures)

The Single-Electron Transistor: The Single-Electron Transistor Single-Electron Transistor Logic, Other SET and FET Structures, Carbon Nano tube Transistors (FETs and SETs), Semiconductor Nano wire FETs and SETs, Molecular SETs and Molecular Electronics.

UNIT-V (11 Lectures)

Spintronics: Basics of magnetism and the origin of magnetism at the atomic scale, Magnetic properties of thin films and nanostructures, Giant magneto resistance (GMR) and tunnel magneto resistance (TMR), Operation principle of magnetic nano-oscillators, Operation principle of spin transistor.

Text Books:

1. Fundamentals of nano electronics by George W Hanson Pearson publications, India 2008.
2. Nano photonics by P.N.Prasad – Springer Education series.
3. Nanotechnology and Nano Electronics – Materials, devices and measurement Techniques by WR Fahrner – Springer
4. Nano materials: Synthesis, properties and applications\edited by A S Edelstein and R C Cammarata (Institute of Physics, UK Series in Micro and Nano science and Technology)

Reference Books:

1. Encyclopaedia of Nano Technology by M.Balakrishna Rao and K.Krishna Reddy (Vol I to X).
2. Nano: The Essentials – Understanding Nano Scinece and Nanotechnology by T.Pradeep; Tata Mc.Graw Hill.
3. Spin Electronics by M. Ziese and M.J. Thornton.
4. Nanoelectronics and Nanosystems – From Transistor to Molecular and Quantum Devices by Karl Goser, Peter Glosekotter, Jan Dienstuhl .
5. Silicon Nanoelectronics by Shunri Odo and David Feny, CRC Press, Taylor & Franicd Group.

6. Nanotubes and nanowires by C.N.R. Rao and A. Govindaraj, RSC Publishing.
7. Encylopedia of Nanotechnology by H.S. Nalwa, American Scientific Publishers.
8. Handbook of Nanoscience, Engineering and Technology by W. Goddard, D. Brenner, S. Lyshevski, G.J.Iafrate, CRC Press (2000).
9. Quantum-Based Electronic Devices and Systems by M. Dutta and M.A. Stroscio, World Scientific.

Web Reference:

1. https://nptel.ac.in/courses/117108047/
2. https://nanohub.org/courses/fon1
3. http://www.tamuk.edu/engineering/departments%20and%20institutes/research/_nano2/index.html
4. https://www.intechopen.com/books/nanoelectronics-and-materials-development
5. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-701-introduction-to-nanoelectronics-spring-2010/index.htm

M.Tech. I Year I Semester

Course Structure

L	T	P	C
3	0	0	3

ASIC DESIGN

(Professional Elective -I)

Internal Marks: 40

Course Code: PP18ECE03 **External Marks: 60**

Course Prerequisite: Basics of VLSI,STLD

Course Objectives:

1. To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
2. To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
3. To gain a knowledge on low level design entry and synthesis for ASIC‘s.
4. To gain knowledge on simulation, partitioning and testing of ASIC’s.
5. To give the student an understanding of placement , routing techniques

Course Outcomes:

On successful completion of this course the students will be able to

1. Student can demonstrate in-depth knowledge in ASIC Design Styles, ASICs Design issues, ASICs Design Techniques, ASIC Construction.
2. Student can analyze the characteristics and Performance of ASICs and judge independently the best suited device for fabrication of smart devices for conducting research in ASIC design.
3. Student is able to give the design entry of devices using HDL’s and able to synthesis them.
4. Student can solve problems of Design issues, simulation and Testing of ASICs.
5. Student can apply appropriate techniques, resources and tools to engineering activities for appropriate Solution to develop ASICs.

UNIT-I (10 Lectures)

Introduction to ASICs:

Types of ASICs- Full-Custom ASICs, Semicustom ASICs, Standard cell based ASICs, Gate- array based ASICs, Channeled Gate Array, Channel less Gate Array, Structured Gate Array, Programmable Logic Devices, Field-Programmable Gate Arrays, ASIC Design Flow.

UNIT-II (9 Lectures)

ASIC Library Design & Programmable ASICs:

ASIC Cell Libraries, , Library cell design, Library Architecture, Gate-Array Design, Standard-Cell Design, Data path-Cell Design. Transistors as Resistors, Transistor Parasitic Capacitance **Programmable ASICS:** Anti fuse, Static RAM, EPROM and EEPROM technology.

UNIT-III (10 Lectures)

Low-Level Design Entry & Logic Synthesis:

Schematic Entry, Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, Vectored instances and Buses, Edit-in-place, Attributes, Net list Screener, Back-Annotation, logic-Synthesis**,** Verilog and Logic Synthesis, VHDL and Logic Synthesis

UNIT-IV (11 Lectures)

Simulation, Testing & ASIC Construction:

Types of Simulation -Structural Simulation, Gate-Level Simulation, Static Timing Analysis, Formal Verification, Switch-Level Simulation, Transistor-Level Simulation, Boundary Scan Test, Faults, Fault simulation, Automatic Test-Pattern Generation

ASIC Construction:

Physical Design, System Partitioning, FPGA Partitioning, Partitioning Methods.

UNIT-V (8 Lectures)

Floor Planning, Placement & Routing:

Floor planning, Placement, Physical Design Flow, Global Routing, Detailed Routing, Special Routing, Circuit Extraction and DRC.

Text Books:

1. M.J.S .Smith, - "Application - Specific Integrated Circuits" – Pearson Education, 2003.

Reference Books:

1. Jose E.France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing", Prentice Hall, 1994.

Website Reference:

1. https://www.radio-electronics.com › Electronic components
2. www.sigenics.com/blog/
3. vlsibyjim.blogspot.com/2015/03/floorplanning.html
4. https://electronics.stackexchange.com/questions/.../floorplanning-vs-placement-in-vlsi

M.Tech. I Year I Semester

Course Structure

L	T	P	C
3	0	0	3

CPLD & FPGA ARCHITECTURES

(Professional Elective -I)

Internal Marks: 40

Course Code: PP18ECE04 **External Marks: 60**

Course Prerequisite: VLSI Design

Course Objectives:

1. Gain a knowledge on different PLD's, CPLD architectures.
2. Gain knowledge on different FPGA architectures and it CLB's.
3. Gain knowledge on SRAM programming technologies of FPGA's.
4. Get an idea on Anti-Fuse Programming technologies of FPGAs
5. Get the practical knowledge of working on a a back end tool ,implementing some designs using tools

Course Outcomes:

On successful completion of this course the

1. Student can understand the concepts of CPLD's and their architectures.
2. Student can understand the concepts of FPGA's and their architectures.
3. Student can perform the SRAM based programming for FPGA's.
4. Student can perform the Antifuse based programming for FPGA's.
5. Student can apply appropriate techniques, Resources and tools in, Modeling complex engineering applications with an understanding of limitations.

UNIT-I (10 Lectures)

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II (10 Lectures)

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

UNIT –III (10 Lectures)

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –IV (9 Lectures)

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT –V (9 Lectures)

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Text Books:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning

Reference Books:

1. P.K.Chan & S. Mourad, “Digital Design Using Field Programmable Gate Array”, jPrentice Hall (Pte), 1994.
2. S.Trimberger, Edr., “Field Programmable Gate Array Technology”, Kluwer Academic Publicatgions, 1994.
3. J. Old Field, R.Dorf, “Field Programmable Gate Arrays”, John Wiley & Sons, Newyork, 1995. 4. S.Brown, R.Francis, J.Rose, Z.

Web Reference:

1. https://www.researchgate.net/.../3250064_FPGA_and_CPLD_architectures_a_tutorial
2. https://www.slideshare.net/sudhirshelke73/unit-vi-cpldfpga-architecture
3. https://www.scribd.com/doc/24072222/m-tech-Cpld-Fpga-Architecture-Applications

M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	1	0	4

SEMICONDUCTOR MEMORY DESIGN AND TESTING

(Professional Elective -II)

Internal Marks: 40

Course Code: PP18ECE05 **External Marks: 60**

Course Prerequisite: Digital Ic Applications

Course Objectives: ·

1. To acquire knowledge on different types of semiconductor memories.
2. To study about architecture and operations of different semiconductor memories.
3. To learn Memory Fault Modeling and Testing
4. To acquire knowledge on Semiconductor Memory Reliability And Radiation Effects
5. To learn about Advanced Memory Technologies And High-Density Memory Packaging Technologies

Course Outcomes:

At the end of the course the student should be able to

1. Understand the different types of RAM, ROM designs.
2. Select architecture and design semiconductor memory circuits and subsystems..
3. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
4. Understand the Memory Reliability And Radiation Effects
5. Identification of new developments in semiconductor memory design.

UNIT-I (10 Lectures)

Random Access Memory Technologies:

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar, SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies- Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and ArchitectureApplication Specific DRAMs.

UNIT-II (10 Lectures)

Non-Volatile Memories:

Masked Read-Only Memories (ROMs)- High Density ROMs-Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating- Gate EPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)- EEPROM Technology And Architecture-Nonvolatile

SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT-III (9 Lectures)

Memory Fault Modeling, Testing, **And Memory Design For Testability And Fault Tolerance**:

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

UNIT-IV (10 Lectures)

Semiconductor Memory Reliability And Radiation Effects:

General Reliability Issues-RAM Failure Modes and Mechanism-Non-volatile Memory Reliability-Reliability Modeling and Failure Rate Prediction Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimeter-Water Level Radiation Testing and Test Structures.

UNIT-V (9 Lectures)

Advanced Memory Technologies And High-Density Memory Packaging Technologies:

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magneto resistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

Text Books :

1. 1.Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ", Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

References Books:

1. Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill.
2. Belty Prince, “ Semiconductor Memory Design Handbook”.
3. Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor (S).

Web Reference :

1. https://books.google.co.in/books?isbn=0780310004
2. https://books.google.co.in/books?id=x1lTAAAAMAAJ

M.Tech. I Year I Semester **Course Structure**

L	T	P	C
3	1	0	4

HARDWARE SOFTWARE CO-DESIGN

(Professional Elective -II)

Internal Marks: 40
Course Code: PP18ECE06 **External Marks: 60**

Course Prerequisite: Embedded Systems

Course Objectives:

1. To do hardware/software co-design for embedded systems.
2. To develop skills in analysis, approach, optimization, and implementation of embedded systems.
3. To exploiting the synergism of hardware and software through their concurrent design.
4. To Develop High-Level Hardware Synthesis Capabilities
5. The Importance Of Codesign Improves Design Quality, Design Cycle Time, And Cost.

Course Outcomes:

Upon the completion of the course student will be able to

1. Understand architectural languages and co-synthesis algorithms for co-design.
2. Understand prototyping and emulation systems and target architectures.
3. Apply compilation tools and techniques for embedded processor architectures.
4. will be able to analysis, design and testing of systems that include both hardware and software.
5. will be able to estimate if additional hardware can accelerate a system.

UNIT –I (9 Lectures)

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT –II (11 Lectures)

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments,

future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), and Mixed Systems.

UNIT –III (8 Lectures)

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV (10 Lectures)

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V (10 Lectures)

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Text Books:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / Software Co- Design Principles and Practice", 2009, Springer.
2. Giovanni De Micheli, Mariagiovanna Sami, "Hardware / Software Co-Design", 2002, Kluwer Academic Publishers

Reference Books:

1. Patrick R.Schaumont, "A Practical Introduction toHardware/Software Co- design", 2010, Springer
2. Jean-Michel Berge (1997), "Hardware/Software Co-Design and Co-Verification", Kluwer Publications.

Web Reference:

1. https://pdfs.semanticscholar.org/presentation
2. http://rijndael.ece.vt.edu/gezel2/book.html
3. https://www.sciencedirect.com/science/book
4. https://dl.acm.org/citation.cfm
5. https://www.kobo.com/us/en/ebook/a-practical-introduction-to-hardware-software-codesign

M.Tech. I Year I Semester

Course Structure

L	T	P	C
3	1	0	4

EMBEDDED NETWORKING

(Professional Elective -II)

Internal Marks: 40

Course Code: PP18ECE07 **External Marks: 60**

Course Prerequisite: Computer Networks, Embedded Systems Design

Course Objectives:

Students undergoing this course are expected to Know basic concepts of embedded Networking

1. Learn about control area network.
2. Learn the network simulation, advanced features and testing of embedded network
3. Know the CAN open standard.
4. Understand the micro CAN open
5. Evaluate the performance of communications protocols used in a networked embedded system

Course Outcomes:

At the end of the course student can able to Analyze embedded Networking applications

1. Apply the concept of CAN in embedded applications like automotives
2. Simulate and test the designed embedded networks
3. Design embedded application using CAN open standard
4. use micro CAN open for designing networking applications

UNIT-I (10 Lectures)

Embedded networking – code requirements – Communication requirements – Introduction to CAN open – CAN open standard. Object directory – Electronic Data Sheets & Device – Configuration files – Service Data Objectives – Network management CAN open messages – Device profile encoder.

UNIT-II (9 Lectures)

CAN open configuration – Evaluating system requirements choosing devices and tools – Configuring single devices.Overall network configuration – Network simulation – Network Commissioning – Advanced features and testing.

UNIT-III (10 Lectures)

Controller Area Network – Underlying Technology CAN Overview – Selecting a CAN Controller – CAN development tools.Implementing CAN open Communication layout and requirements – Comparison of implementation methods.

UNIT-IV (8 Lectures)

Micro CAN open – CAN open source code – Conformance test – Entire design life cycle.Physical layer – Data types – Object dictionary – Communication object identifiers – Emerging objects – Node states.

UNIT-V (11 Lectures)

Ethernet Basics - Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol. Embedded Ethernet - Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure

Text Books:

1. Embedded Networking with CAN and CAN open- GlafP.Feiffer, Andrew Ayre and Christian Keyold, Embedded System Academy 2005.
2. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002.
3. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
4. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003

Reference Books:

1. 1. Principles of Embedded Networked Systems Design-Gregory J. Pottie, William J. Kaiser Cambridge University Press, Second Edition, 2005
2. Rajkamal, ―Embedded Systems Architecture, Programming and Design‖, TATA McGraw-Hill, First reprint Oct. 2003.

Web Reference :

1.http://www.dauniv.ac.in/downloads/EmbsysRevEd_PPTs/Chap_3Lesson17EmsysNew.pdf

M.Tech. I Year I Semester

Course Structure

L	T	P	C
3	1	0	4

ADVANCED OPERATING SYSTEMS

(Professional Elective -II)

Internal Marks: 40

Course Code: PP18ECE08 **External Marks: 60**

Course Prerequisite: computer Architectures& Organization

Course Objectives:

1. To examine the fundamental principles of distributed operating systems
2. To provide hands-on experiences in developing suitable algorithms for distributed system
3. To emphasis on OS resource security and protection and database operating system

Course Outcomes:

At the end of the course, students will be able to:

1. Understand the basic foundation in the design of advanced operating systems.
2. Devise algorithms for distributed file systems, distributed shared memory and distributed scheduling.
3. Assess the basis of the design of advanced operating systems such as failure recovery and fault tolerance.
4. Find the solutions for the problems encountered in the design of advanced operating systems.
5. Analyze algorithms for database operating systems

UNIT I (10 Lectures)

Distributed Operating Systems:

Overview, Synchronization Mechanisms, Architectures of Distributed Systems, Theoretical Foundations. Distributed Mutual Exclusion: Preliminaries, A Simple solution to distributed mutual exclusion, Non-Token Based Algorithm, Lamport's Algorithm, RicartAgrawala algorithm. Distributed Deadlock detection, Agreement Protocols: System Model, Classification of Agreement Problem, solution to byzantine agreement problem.

UNIT II (10 Lectures)

Distributed Resource Management:

Distributed File Systems: Architecture, Mechanisms for building distributed file systems; Distributed Shared memory: Algorithms for implementing

DSM, Memory Coherence, Coherence protocols; Distributed Scheduling – Issues in Load distribution, Components of load distributing algorithm, Load distributing algorithms.

UNIT- III (9 Lectures)

Fault Tolerance:

Failure Recovery and Fault Tolerance-Recovery: Classification of Failures, Backward and forward error recovery, recovery in concurrent systems, Check pointing; Fault Tolerance: Commit protocols, nonblocking commit protocols, voting protocols, dynamic voting protocols, Failure resilient processes.

UNIT- IV (9 Lectures)

Protection And Security:

Protection and Security-Resource Security and protection: Introduction, Preliminaries, Access Matrix Model, Implementation of Access Matrix, safety in Access matrix model. Multiprocessor Operating systems-Multiprocessor System Architectures – Multiprocessor operating systems.

UNIT- V (10 Lectures)

Database Operating Systems:

Database Operating Systems-Introduction to Database Operating systems, Concurrency Control,Theoretical Aspects, Concurrency Control Algorithms – Basic synchronization primitives, lock based algorithms, Timestamp based algorithms.

Text Book:

1.MukeshSinghal, NiranjanG.Shivaratri, Advanced Concepts in Operating Systems: Distributed Database, and Multiprocessor Operating Systems, Tata McGraw-Hill, 2001. ISBN: 0-07-047268-8.

Reference Books:

1. Pradeep K. Sinha, Distributed Operating Systems Concepts and Design, Prentice-Hall of India, 2005, ISBN: 81-203-1380-1
2. Mary Gorman, Todd Stubbs, and Introduction to Operating Systems: Advanced Course, Course Technology, 2001. ISBN: 0619059443.

Web Reference :

1. https://docobook.com/advanced-operating-systems-mukesh-singhal.html
2. https://hpdf.info/read/advanced-concepts-in-operating-systems.pdf
3. https://www.scribd.com/document/331646669/Pradeep-K-Sinha-Distributed-Operating-Systems-Concepts-and-Design-P-K-Sinha
4. https://www.youtube.com/watch?v=MaA0vFKtew&list=PLLDC70psjvq5hIT0kfr1sirNuees0NIbG
5. https://drive.google.com/drive/folders/0B-dwArnVnVKYYTdqeWRNTG1qVkU

M.Tech. I Year I Semester **Course Structure**

L	T	P	C
2	0	0	0

ENGLISH FOR RESEARCH PAPER WRITING

Course code:PP18ECA01: **Internal Marks: 100**
External Marks: -

Course Prerequisite: Nil

Course Objectives:

Students will be able to:

1. Understand that how to improve your writing skills and level of readability
2. Learn about what to write in each section
3. Understand the skills needed when writing a Title

Ensure the good quality of paper at very first-time submission.

UNIT-I (4 Lectures)

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

UNIT-II (4 Lectures)

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.

UNIT-III (4 Lectures)

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

UNIT-IV (4 Lectures)

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature,

UNIT-V (4 Lectures)

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions. useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

References Books:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

M.Tech. I Year I Semester

Course Structure

L	T	P	C
0	0	3	1.5

VLSI LABORATORY

Internal Marks: 40

Course Code: PP18ECL01 **External Marks: 60**

Course Objectives:

1. To learn VHDL for modeling of combinational and sequential circuits.
2. To know the Verification and functionality of designed circuits using functional simulators.
3. To learn the Synthesis procedure of designed circuits.
4. To learn the Implementation of designed circuits using various FPGA kits.

Course Outcomes:

After going through this course the student will be able to

1. Can get the knowledge to implement the digital design on FPGA.
2. Synthesize the encoding techniques by using the Xilinx ISE Simulator.
3. Simulate combinational and sequential circuits using CAD tools.
4. Design digital systems that are reconfigurable for testing and test it on FPGA

Any 10 of The Following Experiments are to be conducted:

PROGRAMS:

1. Parity Encoder.
2. Random Counter
3. Single Port Synchronous RAM.
4. Synchronous FIFO.
5. ALU.
6. UART Model.
7. Dual Port Asynchronous RAM.
8. Fire Detection and Control System using Combinational Logic circuits.
9. Traffic Light Controller using Sequential Logic circuits
10. Pattern Detection using Moore Machine.
11. Finite State Machine (FSM) based logic circuit.
12. Design of 4 bit Multiply and Accumulate unit.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL, Perl Software.

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.

M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	0	0	3

REAL TIME OPERATING SYSTEMS

Internal Marks: 40

Course Code: PP18ECT05 **External Marks: 60**

Course Prerequisite: OS, Embedded System

Course Objective:

To learn

1. Basic concepts Operating Systems
2. Real-time systems and Real-time Operating Systems
3. Design and analysis of computer systems for real-time applications.
4. Resource management, time-constrained communication
5. Initiate research in Real Time Systems
6. Scheduling and imprecise computations, real-time kernels.

Course Outcome:

On completion of the course, students will be knowledgeable in

1. Real-time embedded systems
2. Real time operating system concepts
3. various real-time operating systems.
4. Identifying variable faults in Embedded systems.
5. Commercial RTOS
6. Real time system reference model
7. Real time scheduling approaches

UNIT I (10 Lectures)

Review Of Operating Systems:

Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Introduction to Distributed operating system – Distributed scheduling.

UNIT II (10 Lectures)

Overview Of RTOS:

RTOS Task and Task state - Process Synchronization- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronization problem – Deadlocks

UNIT III (11 Lectures)

Real Time Models And Languages:

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT IV (9 Lectures)

Real Time Kernel:

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target– Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT V **(**8 Lectures)

RTOS Application Domains:

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

Text Books:

1. Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGraw Hill, 2006.
2. Herma K., "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 1997
3. C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill, 1997.

References:

1. Charles Crowley, "Operating Systems-A Design Oriented approach", McGraw Hill 1997.
2. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems", PHI 1999.
3. Mukesh Sighal and N. G. Shi "Advanced Concepts in Operating System", McGraw Hill 2000.

Web Reference :

1. https://cseweb.ucsd.edu/classes/wi13/cse237A-a/handouts/rtos-chap11.pdf
2. http://chettinadtech.ac.in/g_articlen/10-06-28/10-06-28-08-23-52-pratheesh.pdf
3. http://real-time operating systems the engineering of real-time embedded systems book 1
4. real-time embedded components and systems with linux and rtos engineering
5. real-time concepts for embedded systems.
6. real-time systems design principles for distributed embedded applications real-time systems series.

M.Tech. I Year II Semester

Course Structure

L	T	P	C
3	1	0	4

TESTING AND TESTABLITY

Internal Marks: 40

Course Code: PP18ECT06 **External Marks: 60**

Course Prerequisite: Digital Circuits

Course Objectives:

1. To understand different fault models and fault simulation techniques.
2. To understand automatic TG (ATG) for SSFs of Combinational and Sequential circuits.
3. To understand different testability techniques and compression techniques.
4. To understand build in self test (BIST) process, generation and delay fault.
5. To understand System Configuration with Boundary Scan and Boundary Scan Description Language.

Course Outcomes:

After successful completion of the course student will be able to

1. Simulate different simulation techniques.
2. Analyze ATG for SSFs of Combinational and Sequential circuits.
3. Develop different testability techniques and compression techniques.
4. Analyze build in self test (BIST) process, generation and delay fault.
5. Implement System Configuration with Boundary Scan and Boundary Scan Description Language.

UNIT-I (10 Lectures)

Fault Modeling:

Logical Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location, Fault Dominance, Single and Multiple Stuck-Fault Model.

Fault Simulation:

General Fault Simulation Techniques, Fault Simulation for Combinational Circuits, Fault Sampling.

UNIT-II (10 Lectures)

Testing For Single Stuck Faults:

ATG for SSFs in combinational circuits- fault oriented ATG, Fault independent ATG, Random test generation, ATG for SSFs in sequential circuits- TG using iterative array models, Simulation based TG.

UNIT-III (11 Lectures)

Design For Testability:

Testability, Adhoc Design for Testability Techniques, Controllability and Observability by Means of Scan Registers, Generic Scan Based Design.

Compression Techniques - General Aspects of Compression Techniques, Ones-Count Compression, Transition-Count Compression, Parity-Check Compression, Syndrome Testing, Signature Analysis.

UNIT-IV (8 Lectures)

Built-In Self-Test

The Economic Case for BIST, Random Logic BIST, Memory BIST.

UNIT-V (9 Lectures)

Boundary Scan Standard

Motivation, System Configuration with Boundary Scan, Boundary Scan Description Language.

Text Books:

1. M. Abramovici, M.A. Breuer and A.D. Friedman (1996), “Digital Systems and Testable Design", Jaico Publishing House.

Reference Books:

1. M.L. Bushnell and V.D. Agrawal (2002), "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers.

Web References:

1. http://www.pld.ttu.ee/diagnostika/theory/fault.html
2. https://www.ida.liu.se/~zebpe83/teaching/test/lec3.pdf
3. https://www.ida.liu.se/~zebpe83/teaching/test/lec4.pdf
4. https://www.ida.liu.se/~TDTS01/lectures/13/lec9.pdf
5. http://courses.ece.ubc.ca/578/notes5.pdf
6. http://www.cad.t.u-tokyo.ac.jp/~timcheng/NOTES/08_bist_2pp.pdf

M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	1	0	4

WIRELESS SENSOR NETWORKS

Internal Marks: 40

Course Code: PP18ECT07 **External Marks: 60**

Course Prerequisite: Fundamentals of Wireless Networks

Course Objectives:

1. To understand the fundamentals of wireless sensor networks, energy consumption and its gateway concepts.
2. To study the various physical and MAC layers and devices in the layer with its traditional protocols.
3. To study the various network and transport layers and devices in the layer with its traditional protocols.
4. To establish infrastructure with localization and synchronization.
5. Learning WSN including hardware and software development.

Course Outcome:

1. Ability to design & Conduct Experiments, with ad hoc and sensor networks & Interpret data through gateway and analyze energy consumption.
2. Designing of physical layer transceiver with sensing and communication range adapting it appropriate MAC protocol.
3. Designing of routing and congestion entities for transport of data.
4. Designing proper protocols for synchronization and localization.
5. Technical knowhow in building a WSN network with hardware and software and Programming languages.

Unit I (10 Lectures)

Introduction:

Introduction to adhoc/sensor networks: Key definitions of adhoc/ sensor networks, Issues and challenges in design of sensor network, sensor network architecture, data dissemination and gathering, Energy consumption of Sensor nodes, Sensor network scenarios, Optimization goals and figures of merit, Gateway concepts.

Unit II (9 Lectures)

Physical and MAC Layers:

Physical layer and transceiver design considerations in WSNs, Fundamentals of MAC Protocols for wireless sensor networks, SMAC, IEEE 802.15.4.

Unit III (10 Lectures)

Network and Transport Layers:

Routing protocols, Energy-efficient unicast, Broadcast and multicast, Geographic routing, Mobile

nodes, Data-centric and content-based networking, Transport layer and quality of service in wireless sensor network, Coverage and deployment, Reliable data transport, Single packet delivery, Block delivery, Congestion control and rate control.

Unit IV (10 Lectures)

Infrastructure Establishment:

Time Synchronization, Introduction to time synchronization problem, Protocols based on sender receiver synchronization, Protocols based on receiver synchronization, Localization and positioning, Single hop localization and Positioning in multichip environment

Unit V (9 Lectures)

Sensor Network Platforms And Applications:

Sensor node Hardware, Node level software platforms, Node level simulators, Advanced application support, Advanced in-network processing, Application-specific support.

Text Books:

1. Holger Karl & Andreas Willig, " Protocols And Architectures for Wireless Sensor Networks" , John Wiley, 2005.
2. C. Siva Ram Murthy, and B. S. Manoj, "AdHoc Wireless networks ", Pearson Education - 2008.

References Books:

1. Feng Zhao and Leonides Guibas, "Wireless sensor networks ", Elsevier publication - 2004.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, “Wireless Sensor Networks-Technology, Protocols, And Applications”, John Wiley, 2007.

WEB REFERENCE:

1. http://profsite.um.ac.ir/~hyaghmae/ACN/WSNbook.pdf
2. https://people.eecs.berkeley.edu/~prabal/teaching/cs294-11-f05/slides/day21.pdf
3. http://vlab.amrita.edu/index.php?sub=78
4. http://jips.jatsxml.org/Article/11/2/205
5. http://rad.ihu.edu.gr/fileadmin/labsfiles/wireless_communications/DOCUMENTATION/doc_v lab4.pdf

M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	1	0	4

NETWORK SECURITY AND CRYPTOGRAPHY

Internal Marks: 40

Course Code: PP18ECT08 **External Marks: 60**

Course Prerequisite: Fundamental of Computer Protocols

Course Objectives:

1. To understand the fundamentals of computer security.
2. To comprehend and apply authentication services, authentication algorithms.
3. To analyze asymmetric ciphers.
4. To understand the conventional methods of cyber security.
5. To understand the conventional methods of IP security.

Course Outcomes:

1. Interpreting the OSI standard with the layered architecture to provide network security.
2. Building of encryption standards for protecting the networks.
3. Evaluate security mechanisms using rigorous approaches, theoretically.
4. Design a security solution for a given application with respect to cyber security.
5. Ability to protect the current legal issues provide the desired IP security.

Unit I (8 Lectures)

Computer security concepts, OSI security Architecture, Security attacks, Security Services, Security mechanisms, A model for network security.

Unit II (10 Lectures)

Encryption Standards:

Classical Encryption Techniques, Symmetric Cipher Model ,Substitution Techniques, Transposition Techniques ,Rotor Machines, Steganography

Block Cipher Principles: Stream Ciphers and Block Ciphers, Motivation for the Feistel Cipher Structure, The Feistel Cipher, The Data Encryption Standard: DES Encryption, DES Decryption.

Unit III (10 Lectures)

Asymmetric ciphers :

Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, ElGamal cryptosystem, Elliptic Curve Arthimatic, Elliptic Curve Cryptograpy.Number Theory: Prime numbers, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

Unit-IV (9 Lectures)

Cyber security

Cyber security Overview: Security from a global perspectives, Trends and types of attacks and malware, The tpes of malwares, Network and Information Infrastructure Defense overview.

Unit-V (11 Lectures)

IP Security

IP Security Overview: Applications of Ipsec, Benefits of Ipsec, Routing Applications, IPsec Documents IPsec Services ,Transport and Tunnel Modes. IP Security Policy: Security Associations, Security Association Database, Security Policy Database, IP Traffic Processing.

Encapsulating Security Payload: ESP Format, Encryption and Authentication Algorithms, Padding, Anti-Replay Service, Transport and Tunnel Modes

Textbooks:

1. Cryptography & Network Security: Principles and Practices, William Stallings, PEA, Fifth edition
2. Introduction to Computer Networks & Cyber Security, Chwan Hwa Wu, J.David Irwin, CRC press.

References Books:

1. V k Pachghare: Cryptography and Information Security, PHE ,2013.
2. Aaron E. Earle, “Wireless Security Handbook”, Auerbach publications, Taylor & Francis Group, 2006.
3. Yang Xiao and Yi Pan, “Security in Distributed and Networking Systems”, World Scientific, 2007, Chapter 1.

Web Reference:

1. https://nptel.ac.in/syllabus/106105031/
2. www.cse-web.iitkgp.ernet.in/~debdeep/courses_iitkgp/Crypto/index.html
3. http://www.cse.iitm.ac.in/~chester/courses/16e_cns/index.html

M.Tech. I Year II Semester

Course Structure

L	T	P	C
3	0	0	3

IoT & APPLICATIONS

(Professional Elective –III)

Internal Marks: 40

Course Code: PP18ECE09 **External Marks: 60**

Course Prerequisite: Python Programming

Course Objectives:

1. To introduce the Iot terminology, technology and its applications
2. To introduce the raspberry PI platform, that is widely used in IoT applications
3. To introduce the implementation of web based services on IoT devices

Course Outcomes:

1. Understand the new computing technologies
2. Ability to introduce the concept of M2M (machine to machine) with necessary protocols
3. Able to apply the latest computing technologies like cloud computing technology and Big Data
4. Get the skill to program using python scripting language which is used in many IoT devices

UNIT- I (10 Lectures)

Introduction to Internet of Things –Definition and Characteristics of IoT, Physical Design of IoT – IoT Protocols, IoT Communication Models, Iot Communication APIs, IoT enabaled Technologies – Wireless Sensor Networks, Cloud Computing, Big data analytics, Communication protocols, Embedded Systems.

UNIT -II (9 Lectures)

IoT and M2M – Software defined networks, network function virtualization, difference between SDN and NFV for IoT, Basics of IoT System Management with NETCOZF, YANGNETCONF, YANG, SNMP NETOPEER

UNIT- III (10 Lectures)

IoT Programming and interfacing - Introduction to Python - Language features of Python, Introduction to Raspberry PI-Interfaces (serial, SPI, I2C) Programming – Python program with Raspberry PI with focus of interfacing external gadgets, controlling output and reading input from pins.

UNIT- IV (10 Lectures)

IoT Physical Servers and Cloud Offerings – Introduction to Cloud Storage models and communication APIs Webserver – Web server for IoT, Cloud for IoT, Python web application framework Designing a RESTful web API

UNIT-V (9 Lectures)

Case Study & advanced IoT Applications- IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT.

Text Books:

1. Internet of Things - A Hands-on Approach, Arshdeep Bahga and Vijay Madisetti, Universities Press, 2015,
2. Getting Started with Raspberry Pi, Matt Richardson & Shawn Wallace, O'Reilly (SPD), 2014

References Books:

1. Peter Waher, "Learning Internet of Things", PACKT publishing, BIRMINGHAM – MUMBAI
2. The Internet of Things, by Michael Millen, Pearson

Web Reference :

1. https://www.coursera.org/specializations/iot
2. https://www.tutorialspoint.com/internet_of_things/internet_of_things_tutorial
3. https://www.mmh.com/topic/category/iot
4. cseweb.ucsd.edu/classes/wi15/cse237A-a/handouts/8_iot.pdf

M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	0	0	3

ADVANCED DIGITAL SIGNAL PROCESSING
(Professional Elective –III)

Internal Marks: 40

Course Code: PP18ECE10 **External Marks: 60**

Course Prerequisite: Signals and Systems,DSP Architectures

Course Objectives:

1. The student comprehends mathematical description and modelling of discrete time random signals.
2. The student is conversant with important theorems and algorithms.
3. The student learns relevant figures of merit such as power, energy, bias and consistency.
4. The student is familiar with estimation, prediction and filtering concepts and techniques.

Course Outcomes:

1. Simulate spectral estimation algorithms and basic models on computing platform.
2. Introduced discrete time signal processing and characterization of random signals, filter design techniques, and imperfections caused by finite word length.
3. Learn how to estimate the spectra of random signals that are to be processed by a discrete time filter, and to appreciate the performance of a variety of modern and classical spectrum estimation techniques.
4. Learn the theory of modern digital signal processing and digital filter design, including hands-on experience with important techniques involving digital filter design and digital simulation experiments
5. Design AR, MA, ARMA models, Weiner filter, anti aliasing and anti imaging filters, and develop FIR adaptive filter and polyphase filter structures.

Unit-I (10 Lectures)

Introduction and Discrete Fourier Transforms:

Signals, Systems and Processing, Classification of Signals, The Concept of Frequency inContinuous-Time and Discrete-Time Signals, Analog-to-Digital and Digital-to-Analog Conversion, Frequency-Domain Sampling: The Discrete FourierTransform, Properties of the DFT, Linear Filtering Methods Based on the DFT

Unit-II (10 Lectures)

Design of Digital Filters:

General Considerations, Design of FIR Filters, Design of IIR Filters from Analog Filters, Frequency Transformations.

Unit-III (11 Lectures)

Multirate Digital Signal Processing:

Introduction, Decimation by a factor'D', Interpolation by a factor 'I', Sampling rate Conversion by a factor 'I/D', implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion, Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank.

Unit-IV (8 Lectures)

Adaptive Filters:

Applications of Adaptive Filters, Adaptive Direct Form FIR Filters- The LMS Algorithm, Adaptive Direct Form Filters-RLS Algorithm.

Unit-V (9 Lecture**s)**

Fundamentals of Programmable DSPs:

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

Text Books :

1. Proakis and Manolakis, "Digital Signal Processing", Prentice Hall 1996.(fourth edition).
2. Roberto Cristi, "Modern Digital Signal Processing", CengagePublishers, India, (erstwhile Thompson Publications), 2003.
3. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSPMicroprocessors with Examples from TMS320C54xx, cengage Learning India PrivateLimited, Delhi 2012

Reference Books:

1. S.K. Mitra, "Digital Signal Processing: A Computer Based Approach",III Ed, Tata McGraw Hill, India, 2007.
2. E.C. Ifeachor and B W Jarvis, "Digital Signal Processing, a practitioners approach", II Edition, Pearson Education, India, 2002 Reprint.

3. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSPMicroprocessors with Examples from TMS320C54xx, cengage Learning India PrivateLimited, Delhi 2012
4. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture

Web Reference:

1. http://www-syscom.univ-mlv.fr/~zaidi/teaching/dsp-esipe-oc2/Course-Notes__Advanced-DSP.pdf
2. https://lecturenotes.in/subject/362/advanced-digital-signal-processing-adsp
3. https://www.thesisscientist.com/docs/Study%20Notes/38266c62-999b-4bc4-9f4f-329aff5e1c0d
4. https://www.engineering.unsw.edu.au/electrical-engineering/sites/elec/files/u12/outline-elec4621-s1-2013.pdf

M.Tech. I Year II Semester

Course Structure

L	T	P	C
3	0	0	3

PHYSICAL DESIGN AUTOMATION

(Professional Elective –III)

Internal Marks: 40

Course Code: PP18ECE11 **External Marks: 60**

Course Prerequisite: VLSI Design,SoC

Course Objectives:

1. Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
2. Discuss the concepts of design optimization algorithms and their application to physical design automation.
3. Understand the concepts of simulation and synthesis in VLSI Design Automation
4. Formulate CAD design problems using algorithmic methods.
5. understand the concepts of design automation f FPGA'S and MCM'S

Course Outcomes:

Upon the completion of the course student will be able to:

1. Students are able to know how to place the blocks and how to partition the blocks while for designing the layout for IC.
2. Students are able to solve the performance issues in circuit layout.
3. Students are able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing
4. Students are able to decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing
5. Students are able to analyze circuits using both analytical and CAD tools.

UNIT-I (11 Lectures)

VLSI Physical Design Automation - VLSI Design Cycle , Physical Design Cycle, New Trends, Design Styles, System Packaging Styles, Historical Perspectives, Existing Design Tools

Fabrication Process and Its Impact - Fabrication Materials, Fabrication of VLSI Circuits, Design Rules, Layout of the Basic Design, Scaling Methods, Status of Fabrication Process, Issues Related to Fabrication Process, Future of Fabrication Process, Tools and Process Development.

UNIT-II (8 Lectures)

Data Structures and Basic Algorithms - Complexity Issues and NP-hardness, Basic Algorithms, Basic Data Structures, Graph Algorithms for Physical Design.

UNIT-III (11 Lectures)

Partitioning - Introduction to Partitioning, Problem Formulation, Classification of Partitioning Algorithm, Group Migration Algorithm, Simulated Annealing and Evolution, Other Partitioning Algorithm, Performance Drive Partitioning.

Floor planning and Placement - Floor planning, Chip Planning, Pin Assignment, Integrated Approach, Placement.

UNIT-IV (8 Lectures)

Routing and Automation of FPGA's and MCM's - Global Routing, Detailed Routing, Clock Routing, Power and Ground Routing, Compaction, Physical Design Automation of the FPGA's and MCM's.

UNIT-V (10 Lectures)

Chip Input and Output Circuits: ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention.

Text Books:

1. Naveed A. Sherwani (1999), "Algorithms for VLSI Physical Design Automation", Third Edition, Kluwer Academic Publications.

References Books:

1. H.Gerez (1998), "Algorithms for VLSI Design Automation", Wiley Publication.
2. Sadiq M. Sait and Habib Youssef (1999), "VLSI Physical Design Automation:
3. Theory and Practice" by World Scientific Publishers, Singapore/New-Jersey, USA. (Also published by McGraw-Hill Book Co., Europe, December 1995).
4. Algorithms for VLSI Design Automation, S. H. Gerez, Wiley student Edition, JohnWiley and Sons (Asia) Pvt. Ltd,1999.
5. VLSI Physical Design Automation, SungKyu Lim, Springer International Edition.

Web Reference:

1.http://users.ece.utexas.edu/~dpan/PDA_syllabus.pdf
2.https://www.ece.uic.edu/~dutt/courses/ece565/lect-notes.html
3.http://users.ece.utexas.edu/~dpan/EE382V_PDA/

M.Tech. I Year II Semester **Course Structure**

L	T	P	C
3	0	0	3

MOBILE SMART COMMUNICATION DEVICES

(Professional Elective –III)

Internal Marks: 40

Course Code: PP18ECE12 **External Marks: 60**

Course Prerequisite: Cellular and Mobile Communication

Course Objectives:

1. To realise the vision of "Optimally Connected Anywhere, Anytime" supported by all system levels and telecommunication system to service platforms and service.
2. To understand the mobile radio propagation path and the design of mobile radio systems.
3. To understand the aspects of coverage with frequency and time.
4. To understand roaming in order to provide uninterrupted services to complement each other in an optimal communication.
5. To study about evolution of 4G Networks, its architecture and applications.

Course Outcome:

1. General knowledge of Cellular mobile systems and Telecommunication systems.
2. Design and implement various signaling schemes for fading channels.
3. Functional design perceptive for micro and macro level antenna diversity with frequency and time.
4. Conversant use of roaming with various scenarios and diverse technologies.
5. Implement different type of applications for smart phones and mobile devices with latest network strategies.

Unit I (11 Lectures)

Introduction to Cellular Mobile systems: A Basic Cellular System, Performance criteria, Uniqueness of mobile radio environment, Operation of cellular systems, marketing image of hexagonal shaped cells, planning of a cellular system, Analog cellular systems and digital cellular systems.

Telecommunication systems GSM: Mobile Services, System Architecture, Radio interface, Protocols, Localization and calling, Handover, Security, New Data services. DECT: System architecture, Protocol Architecture, TETRA, UMTS and IMT-2000.

Unit II (10 Lectures)

The Mobile-Radio Signal Environment: The Mobile-Radio Communication Medium, Propagation-Path Loss, Multipath Fading Due to Scattering Factors, Thermal Noise and Human-Made Noise Characteristics, Delay Spread, Coherence Bandwidth, Multipath Fading Phenomenon in the 800- to 900-MHz Region.

Unit III (8 Lectures)

Functional Design of Mobile-Radio Systems—Diversity Schemes Microscopic Diversity Schemes—Applied on Cosited Antennas,Space Diversity, Diversity, Polarization, Frequency, Time.

Unit IV (10 Lectures)

Roaming in wireless and Mobile Networks: National and International Roaming, Interstandard Roaming, Prepaid and Postpaid Subscriber Roaming, Basic Structure of Roaming, Roaming Services. Roaming in a GSM Network: Inter-PLMN Signaling Network, Communication between a VPLMN VLR and HPLMN HLR , Roaming Procedures, Roaming call scenarios, Short Message Services(SMS).

Unit V (9 Lectures)

Fundamentals 4G Networks and Composite Radio Environment, Channel Modeling for 4G: Macro cellular Environments, Urban Spatial Radio Channels in Macro/Microcell Environment, MIMO Channels in Micro- and Pico Cell Environment, Outdoor Mobile Channel, Microcell Channel, Wireless MIMO LAN Environments.

Text Books:

1. W.C.Y.Lee, "Mobile Cellular Telecommunications - Analog and Digital Systems", 2nd Edition. Tata McGraw Hill, 2006.
2. J. Schiller, "Mobile Communications", Pearson Education.
3. William C. Y. Lee: Mobile Communications Engineering: Theory and Applications, Second Edition.

Reference:

1. Glisic, Savo G., Advanced Wireless Networks, John Wiley and Sons (2006).
2. Shahid K. Diddiqui, "Roaming in Wireless Networks", McGraw Hill Professional

Web Reference :

1. https://www.cse.wustl.edu/~jain/refs/wir_refs.htm
2. https://www.tech.ihu.edu.gr/index.php/en/research/item/30-virtual-labs.html
3. http://fcmcvlab.iitkgp.ac.in/
4. https://whatsag.com/g/understanding_4g.php

M.Tech. I Year II Semester

Course Structure

L	T	P	C
3	1	0	4

IMAGE & VIDEO PROCESSING

(Professional Elective –IV)

Internal Marks: 40

Course Code: PP18ECE13 **External Marks: 60**

Course Prerequisite: Digital Image Processing

Course Objectives:

The student will

1. Learn the fundamental concepts and applications of Digital Image Processing.
2. Learn the concepts of and how to perform Intensity transformations and spatial filtering. Understand the concepts of and how to perform Image restoration and reconstruction.
3. Understand the concepts of Image Segmentation and Compression used in digital image processing
4. Able to expose the students to current applications, techniques and issues in image and video processing.
5. Able to develop image and video processing applications in practice.

Course Outcomes:

After going through this course the student will be able to

1. Perform different transforms on image useful for image processing applications
2. Perform spatial and frequency domain filtering on image and can implement all smoothing and sharpening operations on images and image restoration operations/techniques on images
3. Categorize various compression techniques and standards. Image segmentation and representation techniques.
4. Understand different methods, models for video processing and motion estimation.
5. Apply quantitative models of image and video processing for various engineering applications and develop innovative design for practical applications in various fields

UNIT –I (10 Lectures)

Fundamentals of Image Processing and Image Transforms:

Origins of Digital Image Processing, Uses Digital Image Processing, Fundamental steps in Digital Image Processing, Components of an Image Processing System, Image Sampling and Quantization, Some Basic Relationships between Pixels. Need for image transforms, 2 D Discrete Fourier transform and its transforms, Walsh transform, Hadamard transform, Haar transform, Slant transform, Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT –II (9 Lectures)

Image Enhancement:

Histogram processing, Fundamentals of Spatial and Frequency domain filtering, Smoothing and Sharpening filters in Spatial and Frequency domain,

Image Restoration:

Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution.

UNIT –III (10 Lectures)

Image Segmentation:

Introduction to image segmentation, Point, Line and Edge Detection, Region based segmentation., Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour.

Image Compression:

Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon –Fano coding, Huffman coding, Arithmetic coding, Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression, JPEG Standards.

UNIT –IV (9 Lectures)

Basic Steps of Video Processing: Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V (10 Lectures)

2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion

estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

Text Books:

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.

2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

3. S.Jayaraman, S.Esakkirajan and T.VeeraKumar, "Digital Image processing, Tata Mc Graw Hill publishers, 2009.

Reference Books:

1. Digital Image Processing and Analysis-Human and Computer Vision Application with CVIP Tools – Scotte Umbaugh, 2nd Ed, CRC Press, 2011.
2. Digital Video Processing – M. Tekalp, Prentice Hall International.
3. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar – TMH, 200911
4. Multidimentional Signal, Image and Video Processing and Coding – John Woods, 2nd Ed, Elsevier.
5. Digital Image Processing with MATLAB and Labview – Vipula Singh, Elsevier.
6. Video Demystified – A Hand Book for the Digital Engineer – Keith Jack, 5th Ed., Elsevier

Web Reference:

1. https://www.sciencedirect.com/science/book/9780121197926
2. http://www.commsp.ee.ic.ac.uk/~tania/teaching/DIP.html
3. https://www.eee.hku.hk/~elec4245/sp17/lec5-2x2.pdf
4. https://en.wikipedia.org/wiki/Video_processing
5. http://www.mee.tcd.ie/~sigmedia/pmwiki/uploads/Teaching.4S1b/handout8_4s1.pdf

M.Tech. I Year II Semester

Course Structure

L	T	P	C
3	1	0	4

EMBEDDED DEVICE DRIVERS

(Professional Elective –IV)

Internal Marks: 40

Course Code: PP18ECE14 **External Marks: 60**

Course Prerequisite: Micro Processors and Micro Controllers

Course Objectives: ·

1. To know about the Device Drivers need and loadable modules
2. To Learn the debugging techniques and Advanced char driver operations
3. To Learn the Concurrency and Race Conditions
4. To Understand fundamentals of hardware interface with kernel
5. To acquire knowledge on interrupt handling and kernel data types

Course Outcomes:

Upon the completion of this course students will be able to:

1. Understands the Device Drivers need and loadable modules
2. Learn the debugging techniques and Advanced char driver operations
3. Understand Concurrency and Race Conditions
4. Understand fundamentals of hardware interface with kernel
5. Use and get acquaint to interrupt handling and kernel data types

UNIT-I (10 Lectures)

An Introduction to Device Drivers:

The Role of the Device Driver, Splitting the Kernel, Classes of Devices and Modules, Security Issues, Version Numbering

Building and Running Modules:

Setting Up Your Test System, The Hello World Module, Kernel Modules Versus Applications, Compiling and Loading, The Kernel Symbol Table, Preliminaries, Initialization and Shutdown, Module Parameters, Doing It in User Space

UNIT-II (10 Lectures)

Char Drivers:

The Design of scull, Major and Minor Numbers, Some Important Data Structures, Char Device Registration, open and release, scull's Memory Usage, read and write, Playing with the New Devices.

Debugging Techniques:

Debugging Support in the Kernel, Debugging by Printing, Debugging by Querying, Debugging by Watching, Debugging System Faults, Debuggers and Related Tools.

UNIT-III (10 Lectures)

Concurrency and Race Conditions:

Pitfalls in scull, Concurrency and Its Management, Semaphores and Mutexes, Completions, Spinlocks, Locking Traps, Alternatives to Locking

Advanced Char Driver Operations:

Octl, Blocking I/O, poll and select, Asynchronous Notification, Seeking a Device, Access Control on a Device File.

UNIT-IV (9 Lectures)

Time, Delays, and Deferred Work:

Measuring Time Lapses, Knowing the Current Time, Delaying Execution, Kernel Timers, Tasklets, Work queues

Allocating Memory:

The Real Story of kmalloc, Look aside Caches, get_free_page and Friends, vmalloc and Friends, Per-CPU Variables, Obtaining Large Buffers

Communicating with Hardware - I/O Ports and I/O Memory, Using I/O Ports, An I/O Port Example, Using I/O Memory.

UNIT-V (9 Lectures)

Interrupt Handling:

Preparing the Parallel Port, Installing an Interrupt Handler, Implementing a Handler, Top and Bottom Halves, Interrupt Sharing, Interrupt-Driven I/O

Data Types in the Kernel:

Use of Standard C Types, Assigning an Explicit Size to Data Items, Interface-Specific Types, Other Portability Issues, Linked Lists.

Text Books:

1. Jonathan Corbet, Alessandro Rubini, and Greg Kroah-Hartman (2005), "Linux Device Drivers" O'Reilly Third Edition

Reference Books:

1. Robert Love, "Linux Kernel Development", 3rd Edition, Addison-Wesley Professiona.
2. Sreekrishnan Venkateswaran, "Essential Linux Device Drivers", Prentice Hall

Web Reference :

1. https://www.coursera.org/lecture/iot-architecture/device-drivers-AL7YG

M.Tech. I Year II Semester

Course Structure

L	T	P	C
3	1	0	4

VLSI SIGNAL PROCESSING

(Professional Elective –IV)

Internal Marks: 40

Course Code: PP18ECE15 **External Marks: 60**

Course Prerequisite: DSP

Course Objectives:

1. Introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications.
2. Design and optimize VLSI architectures for basic DSP algorithms.
3. To make an in depth study of DSP structures amenable to VLSI implementation.
4. To enable students to design VLSI system with high speed and low power.
5. To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
6. To introduce efficient design of DSP architectures suitable for VLSI

Course Outcomes:

1. Understand VLSI design methodology for signal processing systems.
2. Familiar with VLSI algorithms and architectures for DSP.
3. Able to implement basic architectures for DSP using CAD tools.
4. Ability to modify the existing or new DSP architectures suitable for VLSI.
5. Be able to make use of Transformation Techniques.

Unit I (10 Lectures)

Introduction To DSP Systems:

Introduction; representation of DSP algorithms: Block Diagram, signal flow graph, data flow graph, dependence graph. Iteration Bound: Data flow graph representations, loop bound and iteration bound, longest path matrix algorithm, iteration bound of Multirate data flow graphs.

Unit II (10 Lectures)

Pipelining and Parallel Processing:

Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

Unit III (10 Lectures)

Unfolding:

Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.

Unit IV (9 Lectures)

Systolic Architecture Design:

Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

Unit V (9 Lectures)

Fast Convolution:

Introduction, Cook, Toom Algorithm, Winogard Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Textbooks:

1. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-Inter Sciences, 1999
2. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill, 1994.
3. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern singal processing, Prentice Hall, 1985.

References:

1. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing' Prentice Hall, 1994.
2. Keshab k. Parhi," VLSI Digital Signal Processing Systems: Design and Implementation", Wiley, inter science. REFERENCE BOOKS 1.S.Y.kung, H.J.White house, T. Kailath," VLSI and Modern Signal Processing", Prentice hall,

Web Reference:

1. http://www.ece.ucdavis.edu/~bbaas/281/notes/Lecture01.pdf\
2. https://drive.google.com/file/d/0BzoKWH8M1BoTb1d4SVNFSlZMdHM/view
3. https://drive.google.com/file/d/0BzoKWH8M1BoTdUpldzR3QkY3QlU/view

L	T	P	C
3	1	0	4

ARTIFICIAL INTELLIGENCE

(Professional Elective –IV)

Internal Marks: 40

Course Code: PP18ECE16 **External Marks: 60**

Course Prerequisite: Mathematics

Course Objectives:

1. To understand artificial intelligence with various models.
2. To understand supervised learning models.
3. To understand unsupervised learning models.
4. To understand the level for randomness in fuzzy sets.
5. To analyse unconstrained optimization techniques.

Course Outcome:

1. Apply artificial intelligence techniques to solve engineering problem.
2. Handling supervised learning with proper training set.
3. Handling unsupervised learning without training set.
4. Creating membership functions for quantifying the amount of randomness.
5. Incorporating unconstrained optimization in to solve engineering problems.

UNIT-1 (9 Lectures)

Introduction to Artificial Neural Networks:

Fundamental concepts: Artificial neural networks, Biological neural networks, Brain versus computer, Basic model of artificial neural network, Important Technologies of artificial neural network, McCulloch-Pitts Model.

UNIT-II (10 Lectures)

A Survey of Neural Network Models: supervised learning

Perception model, ADALINE (Adaptive Linear neuron)-algorithm : Theory, Architecture, Flowchart of training process, Training algorithm, Testing algorithm, Multiple Adaptive Linear neuron MADALINE-algorithm Theory, Architecture, Flowchart of training process, Training algorithm, Testing algorithm. Back propagation networks Theory, Architecture, Flowchart of training process, Learning factors of Back propagation networks, Testing algorithm of Back propagation networks.

UNIT-III (10 Lectures)

A Survey of Neural Network Models: unsupervised learning

Kohonen Self organizing Feature map: Theory, Architecture, Flowchart, Training Algorithm, Kohonen Self organizing map. Learning Vector Quantization: Theory, Architecture, Flowchart, Training Algorithm, Variants. Counter propagation networks: Theory, Full counter propagation Net, Forward only counter propagation Net. Adaptive Resonance theory.

UNIT-IV (10 Lectures)

Fuzzy sets

Classical Sets : Operations on Classical Sets, Properties of Classical (Crisp) Sets, Mapping of Classical Sets. Fuzzy Sets Fuzzy Set Operations, Properties of Fuzzy Sets, Alternative Fuzzy Set Operation. Properties of Membership Functions, Fuzzification, and Defuzzification Features of the Membership

Function, Various Forms, Fuzzification, Defuzzification to Crisp Sets, λ-Cuts for Fuzzy Relations, Defuzzification to Scalars.

UNIT-V (9 Lectures)

Optimization Techniques

Unconstrained Optimization: Basics of set constrained and unconstrained optimization. One dimensional search methods. Gradient method, Newton method, Conjugate direction methods, Quasi newton methods. Global search algorithms: Simulated annealing, Particle swarm optimization and Genetic algorithm.

Textbooks:

1. Principles of Soft Computing by S. N. Sivanandam, S. N. Deepa, Wiley-India.
2. Neural Networks Fuzzy Logic & Genetic Alogrithms by Rajshekaran & Pai, Prentice Hall.

References :

1. Fuzzy Logic with Engineering Applications., McGraw Hill,Second edition Ross T.J.,
2. An Introduction to Optimization Edwin K., P. Chong & Stanislaw h. Zak

Web Reference :

1.http://vlabs.iitkgp.ernet.in/scte/

2. http://cse22-iiith.vlabs.ac.in/

3. https://swayam.gov.in/course/4574-introduction-to-soft-computing.

4. https://www.hindawi.com/journals/mpe/soft.computing/

5.https://in.mathworks.com/products/optimization.html?requestedDomain

M.Tech. I Year II Semester **Course Structure**

L	T	P	C
2	0	0	0

Personality Development through Life Enlightenment Skills

Internal Marks: 100
Course Code: PP18ECE16 **External Marks: -**

Course Objectives:

1. To learn to achieve the highest goal happily.
2. To become a person with stable mind, pleasing personality and determination.
3. To awaken wisdom in students.

Course Outcomes:

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life
2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity
3. Study of Neetishatakam will help in developing versatile personality of students.

UNIT-I (4 Lectures)

Neetisatakam-Holistic development of personality

- Verses- 19,20,21,22 (wisdom)
- Verses- 29,31,32 (pride & heroism)
- Verses- 26,28,63,65 (virtue)

UNIT-II (4 Lectures)

Neetisatakam-Holistic development of personality

- Verses- 52,53,59 (dont's)
- Verses- 71,73,75,78 (do's)

UNIT-III (4 Lectures)

Approach to day to day work and duties.

Shrimad BhagwadGeeta :

Chapter 2-Verses 41, 47,48

Chapter 3-Verses 13, 21, 27, 35

Chapter 6-Verses 5,13,17, 23, 35

Chapter 18-Verses 45, 46, 48.

UNIT-IV (4 Lectures)

Statements of basic knowledge.

Shrimad BhagwadGeeta:

Chapter2-Verses 56, 62, 68

Chapter 12 -Verses 13, 14, 15, 16,17, 18

UNIT-V (4 Lectures)

Personality of Role model.

Shrimad BhagwadGeeta:

Chapter2-Verses 17,

Chapter 3-Verses 36,37,42,

Chapter 4-Verses 18, 38,39

Chapter18 – Verses 37,38,63

Suggested reading

1. “Srimad Bhagavad Gita” by Swami SwarupanandaAdvaita Ashram (Publication

2. Department), Kolkata

3. Bhartrihari’s Three Satakam (Niti-sringar-vairagya) by P.Gopinath,

4. Rashtriya Sanskrit Sansthanam, New Delhi.

M.Tech. I Year II Semester

Course Structure

L	T	P	C
0	0	3	1.5

EMBEDDED SYSTEM DESIGN LABORATORY

Internal Marks: 40

Course Code: PP18ECL02 **External Marks: 60**

Course Objectives:

1. To learn about creating new command and allocating resources by using semaphores and mutex.
2. To know about avoiding deadlock using bankers algorithm and synchronize identical threads.
3. To learn the implementation and interfacing of display with ARM-CORTEX processor and can simulate the temperature with SERIAL communication PC.
4. To implement developers board for data communication using serial port communication.

Course Outcomes:

After completing these experiments students can able to;

1. Create their own tasks with ARM-926 board.
2. Handle errors and create algorithms.
3. Identify writer's and reader's errors and can handle.
4. Interface and simulate with serial communication with PC.
5. Develop communication between different PC's.

The students are required to perform at least SIX experiments from Part - I and TWO experiments from Part-II.

List of Experiments:

Part-I: Experiments using ARM-926 with Perfect RTOS

1. Register a new command in CLI.
2. Interrupt handling.
3. Allocate resource using semaphores.
4. Share resource using MUTEX.
5. Avoid deadlock using BANKER'S algorithm.
6. Synchronize two identical threads using MONITOR.
7. Reader's Writer's Problem for concurrent Tasks.

Part-II Experiments on ARM-CORTEX processor using any open source RTOS.

(Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Simulate the temperature DATA Logger with the SERIAL communication with PC.
3. Implement the developer board as a modem for data communication using serial port communication between two PC's.

Lab Requirements:

Software:

Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER. LINUX Environment for the compilation using Eclipse IDE & Java with latest version.

HARDWARE:

The development kits of ARM-926 Developer Kits and ARM-Cortex Boards. Serial Cables, Network Cables and recommended power supply for the board.

M.Tech. II Year I Semester **Course Structure**

L	T	P	C
2	0	0	2

RESEARCH METHODOLOGY AND IPR

Internal Marks: -

Course Code: PP18MCT01 **External Marks: -**

Course Prerequisites: Nil

Course Objectives:

1. understand some basic concepts of research and its methodologies
2. identify appropriate research topics
3. select and define appropriate research problem and parameters
4. prepare a project proposal (to undertake a project)
5. organize and conduct research (advanced project) in a more appropriate manner.
6. The main objective of the IPR is to make the students aware of their rights for the protection of their invention done in their project work.

Course Outcomes:

At the end of this course, students will be able to

1. Understand research problem formulation.
2. Analyze research related information
3. Follow research ethics
4. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
6. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT- I (4 Lectures)

Meaning of research problem, Sources of research problem, Criteria
Characteristics of a good research problem, Errors in selecting a research problem, Scopen and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis,
interpretation, Necessary instrumentations.

UNIT-II (4 Lectures)

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT-III (4 Lectures)

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-IV (4 Lectures)

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology.
Patent information and databases. Geographical Indications.

UNIT-V (4 Lectures)

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction
3. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

References Books:

1. Ranjit Kumar, 2 ndEdition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in NewTechnological Age", 2016.

Web Reference :

1. https://www.isical.ac.in/~palash/research-methodology/RM-lec4.pdf\
2. http://www.bitspilani.ac.in/uploads/Patent_ManualOct_25th_07.pdf
3. https://my.cumbria.ac.uk/media/MyCumbria/IPR-notes-and-guidance.pdf